1. A method of defining a conductive gate structure for a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate, comprising the steps of:

providing a gate insulator layer on said semiconductor substrate;

forming a conductive layer on said gate insulator layer;

forming a capping insulator layer on said conductive layer;

forming a dielectric anti-reflective coating (DARC) layer on said capping insulator layer;

forming a patterned photoresist shape on said DARC layer;

performing a first phase of a first dry etch procedure using said photoresist shape as an etch mask to define a first stack comprised of said photoresist shape and a DARC shape;

performing a second phase of said first dry etch procedure using said photoresist shape as an etch mask to define a capping insulator shape underlying said first stack;

removing said photoresist shape resulting in a second stack comprised of said DARC shape and said capping insulator shape;

performing a second dry etch procedure using said second stack as an etch mask to define a conductive gate structure and to remove said DARC shape; and

performing a wet etch procedure to remove portions of said gate insulator layer not covered by said conductive gate structure and to remove said capping insulator layer.

2. The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer at a thickness between about 6 to 80 Angstroms.

3. The method of claim 1, wherein said conductive layer is a polysilicon layer at a thickness between about 400 to 1800 Angstroms, wherein a polysilicon layer is either doped in situ during deposition via the addition of arsine or phosphine to a silane ambient, or wherein a polysilicon layer is deposited intrinsically then doped via implantation of arsenic or phosphorous ions.

4. The method of claim 1, wherein said conductive layer is a metal silicide layer such as a tungsten silicide layer.

5. The method of claim 1, wherein said capping insulator layer is a silicon oxide layer obtained at a thickness between about 100 to 400 Angstroms via LPCVD or via plasma enhanced chemical vapor deposition (PECVD) procedures.

6. The method of claim 1, wherein said DARC layer is a silicon oxynitride (SiON) layer obtained at a thickness between about 200 to 600 Angstroms, via PECVD procedures.

7. The method of claim 1, wherein said DARC layer is a silicon nitride layer.

8. The method of claim 1, wherein said organic bottom anti-reflective coating (BARC), at a thickness between about 500 to 1200 Angstroms, is formed on said DARC layer.

9. The method of claim 1, wherein said photoresist shape is comprised with a width between about 1500 to 4000 Angstroms.

10. The method of claim 1, wherein said first phase of a first dry etch procedure used to define said first stack comprised of said photoresist shape, a BARC shape, and said DARC shape, is an anisotropic reactive ion etch (RIE) procedure performed using CF_4 CHF_3, CH_2F_2, HBR, O_2 and N_2 as etchants.

11. The method of claim 1, wherein said second phase of said first dry etch procedure used to define said capping insulator shape, is anisotropic reactive ion etch (RIE) procedure performed using a fluorine based chemistry comprised with either CHF_3, CH_3F, CH_2F_2, or CF_4 as an etchant.

12. The method of claim 1, wherein said photoresist shape and a BARC shape are removed via plasma oxygen ashing procedures.

13. The method of claim 1, wherein said second dry etch procedure used to define said conductive gate structure and to remove said DARC shape, is an anisotropic RIE procedure using an etch chemistry comprised of Cl_2, HBR, and CF_4 as etchants.

14. The method of claim 1, wherein said wet etch procedure used to remove portions of said gate insulator layer not covered by said conductive gate structure and to remove said capping insulator shape, is performed using either a dilute hydrofluoric (DHF) or a buffered hydrofluoric (BHF) acid solution.

15. A method of defining a polysilicon gate structure for a (MOSFET) device on a semiconductor substrate using dual anti-reflective coating (ARC) layers, and featuring dry etch removal of a dielectric ARC component, comprising the steps of:

providing a silicon dioxide gate insulator layer on said semiconductor substrate;

forming a polysilicon layer on said silicon dioxide gate insulator layer;

forming a capping silicon oxide layer on said polysilicon layer;

forming a dielectric anti-reflective coating (DARC) layer on said capping silicon oxide layer;

forming an organic bottom anti-reflective coating (BARC) layer on said DARC layer;

forming a photoresist shape on said BARC layer;

performing a first phase of a first anisotropic reactive ion etching (RIE) procedure using said photoresist shape as an etch mask, to define a first stack comprised of said photoresist shape, a BARC shape, and a DARC shape;

performing a second phase of said first anisotropic RIE procedure using said photoresist shape as an etch mask, to define a capping silicon oxide shape underlying said first stack;

removing said photoresist shape and said BARC shape resulting in a second stack comprised of said DARC shape and said capping silicon oxide shape;

performing a second anisotropic RIE procedure using said second stack as an etch mask to define said polysilicon gate structure and to remove said DARC shape; and

performing a wet etch procedure to remove portions of said silicon dioxide gate insulator layer not covered by said polysilicon gate structure, and to remove said capping silicon oxide layer.

16. The method of claim 15, wherein said silicon dioxide gate insulator layer is obtained at a thickness between about 6 to 80 Angstroms.

17. The method of claim 15, wherein said polysilicon layer is obtained at a thickness between about 400 to 1800 Angstroms, wherein a polysilicon layer is either doped in situ during deposition via the addition of arsine or phosphine to a silane ambient, or deposited intrinsically then doped via implantation of arsenic or phosphorous ions.

18. The method of claim 15, wherein said capping silicon oxide layer is obtained at a thickness between about 100 to 400 Angstroms via LPCVD or via plasma enhanced chemical vapor deposition (PECVD) procedures.

19. The method of claim 15, wherein said DARC layer is a silicon oxynitride (SiON) layer obtained at a thickness between about 200 to 600 Angstroms, via PECVD procedures.

20. The method of claim 15, wherein said DARC layer is a silicon nitride layer.

21. The method of claim 15, wherein said BARC layer is applied at a thickness between about 500 to 1200 Angstroms.

22. The method of claim 15, wherein said photoresist shape is comprised with a width between about 1500 to 4000 Angstroms.

23. The method of claim 15, wherein said first phase of said first anisotropic RIE procedure used to define said first stack comprised of said photoresist shape, said BARC shape, and said DARC shape, is performed using a chemistry comprised with CF_4, CHF_3, CH_2F_2, HBR, O_2 and N_2 as etchants.

24. The method of claim 15, wherein said second phase of said first anisotropic RIE procedure used to define said capping insulator shape, is performed using a fluorine based chemistry comprised with either CHF_3, CF_4, CH_2F_2, and CH_3F as etchants.

25. The method of claim 15, wherein said photoresist shape and BARC shape are removed via plasma oxygen ashing procedures.

26. The method of claim 15, wherein said second anisotropic RIE procedure, used to define said conductive gate structure and to remove said DARC shape, is performed using Cl_2, HBR, and CF_4 as etchants.

27. The method of claim 15, wherein said wet etch procedure used to remove portions of said silicon dioxide gate insulator layer not covered by said polysilicon gate structure, and to remove said capping silicon oxide shape, is performed using either a dilute hydrofluoric (DHF) or a buffered hydrofluoric (BHF) acid solution.